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Claims

[c1] An interlevel dielectric layer comprising:
a dielectric layer; and
a dielectric film, deposited under compressive stress,
atop the dielectric layer.

[c2] The interlevel dielectric layer, according to claim 1,
wherein the dielectric layer comprises a low-k material.

[c3] The interlevel dielectric layer, according to claim 1,
wherein the dielectric layer comprises
an organosilicon glass.

[c4] The interlevel dielectric layer, according to claim 1,
wherein the dielectric layer comprises a SiCOH material.

[c5] The interlevel dielectric layer, according to claim 1,
wherein:
the dielectric layer has a thickness of 500 - 20,000 Å
and
the dielectric film has a thickness of 200 - 2000 Å.

[c6] The interlevel dielectric layer, according to claim 1,
wherein:
the dielectric layer has a thickness of 1000 - 15,000 Å

and
the dielectric film has a thickness of 350 - 1000 Å.

[c7] The interlevel dielectric layer, according to claim 1, wherein the dielectric film has a thickness which is 2% - 10% of the thickness of the dielectric layer.

[c8] The interlevel dielectric layer, according to claim 1, wherein the dielectric film has a thickness which is approximately 3% of the thickness of the dielectric layer.

[c9] The interlevel dielectric layer, according to claim 1, wherein the dielectric film has similar chemical composition to the dielectric layer, but has different morphology than the dielectric layer.

[c10] The interlevel dielectric layer, according to claim 1, wherein a dielectric cap is deposited on the dielectric film.

[c11] A method of forming an interlevel dielectric layer comprising the steps of:
depositing a low-k dielectric layer; and
depositing a low-k dielectric film under compressive stress at or near the end of the low-k dielectric layer deposition.

[c12] The method, according to claim 11, including the step of

depositing the low-k dielectric film by altering a process used to deposit the low-k dielectric layer.

[c13] The method, according to claim 11, including the step of depositing the low-k dielectric layer and the low-k dielectric film using a CVD process.

[c14] The method, according to claim 11, including the step of depositing the low-k dielectric film in situ with the low-k dielectric layer.

[c15] The method, according to claim 11, including the step of depositing the low-k dielectric layer and the low-k dielectric film using a CVD process and a tetramethylcyclotetrasiloxane precursor material.

[c16] The method, according to claim 11, including the steps of:
depositing the low-k dielectric layer using a spin-on process; and
depositing the low-k dielectric film using a CVD process.

[c17] The method, according to claim 11, including the step of using the low-k dielectric film as a polish stop layer during copper chemical mechanical polishing.

[c18] The method, according to claim 11, further comprising the steps of:

forming damascene copper interconnects in the inter-level dielectric layer;

chemical mechanical polishing the resulting structure; and

depositing a dielectric cap on the resulting structure.

[c19] The method, according to claim 18, wherein the dielectric cap is under compressive stress.